Claims

- [c1] A method of testing an integrated circuit structure comprising the steps of:

 providing a semiconductor wafer containing a set of chip locations for forming a set of integrated circuits therein; fabricating in said wafer a set of transistors specific to a particular integrated circuit in said chip locations; connecting at least one subset of transistors by a lithographic process in at least one chip location in a test interconnect arrangement using interconnect levels close to said semiconductor material; and testing at least one parameter of said subset of transistors.
- [c2] A method according to claim 1, in which said test arrangement is constructed using only a first interconnect level above said set of transistors.
- [c3] A method according to claim 1, in which said test arrangement is constructed using both a first and second interconnect level above said set of transistors.
- [c4] A method according to claim 1, in which said subset is a portion of an integrated circuit.

- [c5] A method according to claim 1, in which said subset is a subcircuit module of an integrated circuit.
- [c6] A method according to claim 2, in which said subset is a subcircuit module of said integrated circuit.
- [c7] A method according to claim 1, in which said subset comprises at least two subcircuit modules of said integrated circuit.
- [c8] A method according to claim 1, in which said test comprises providing an input test vector and recording output signals from said test structure.
- [c9] A method according to claim 1, further comprising a step of removing said test interconnect arrangement and depositing an interconnect layer of said integrated circuit in replacement thereof.
- [c10] A method according to claim 9, in which said test arrangement is constructed using only a first interconnect level above said set of transistors.
- [c11] A method according to claim 9, in which said test arrangement is constructed using both a first and second interconnect level above said set of transistors.
- [c12] A method according to claim 9, in which said subset is a

- portion of an integrated circuit.
- [c13] A method according to claim 9, in which said subset is a subcircuit module of an integrated circuit.
- [c14] A method according to claim 10, in which said subset is a subcircuit module of said integrated circuit.
- [c15] A method according to claim 9, in which said subset comprises at least two subcircuit modules of said integrated circuit.
- [c16] A method according to claim 9, in which said test comprises providing an input test vector and recording output signals from said test structure.
- [c17] A method of manufacturing integrated circuits with an integrated circuit process comprising the steps of: providing a set of semiconductor wafers containing a set of chip locations for forming a set of integrated circuits therein;

fabricating a set of transistors specific to a particular integrated circuit in said wafers in said chip locations; connecting at least one subset of transistors by a lithographic process in at least one chip location in a test interconnect arrangement using interconnect levels close to said semiconductor material;

testing at least one parameter of said subset of transis-

tors; and modifying a step in said integrated circuit process when a parameter of said subset of transistors is out of specification.

- [c18] A method according to claim 17, in which said test arrangement is constructed using only a first interconnect level above said set of transistors.
- [c19] A method according to claim 17, in which said test arrangement is constructed using both a first and second interconnect level above said set of transistors.
- [c20] A semiconductor wafer containing a set of chip locations for forming a set of integrated circuits therein; each of said set of chip locations having a set of transistors specific to a particular integrated circuit in said wafer in said chip locations, wherein at least one chip location has a subset of transistors connected by a lithographic process in a test interconnect arrangement, different from a circuit interconnect arrangement, using interconnect levels close to said semiconductor material.